DFT FOR MODERN MANAGERS

Overview

A 2-day intensive training designed for managers and program leads to gain strategic and technical insights into Design-for-Test (DfT) and broader DfX concepts.

Learn how to engage effectively with design and test teams, evaluate trade-offs, and make informed decisions that optimize yield, cost, and time-to-market.

📌 Tailored for leadership roles, the course blends lectures, case studies, walkthroughs, and group discussions.

Target Audience

- Engineering Managers
- Program Managers
- Technical Project Leads
- Product Owners

OBJECTIVES

By the end of this course, participants will be able to:

- Understand DfT techniques for semiconductor devices
- Recognize the strategic importance of DfT in product development
- Apply industry standards (IEEE 1149.1/1500/1687)
- Manage ATPG, MBIST, scan, and boundary scan
- Interface effectively with product development teams
- Analyze real product scenarios through hands-on case discussions

FORMAT & DELIVERY

- **Duration:** 2 full days
- **Mode:** On-site or remote (customizable per team)
- **Style:** Lectures, visual walkthroughs, case studies, group activities
- **Customization:** Aligned with your existing tools, workflows, and project context

BUILD SMARTER TEST STRATEGIES

COURSE CURRICULUM

Day 1: DfT Concepts & Strategic Relevance

- Introduction to DfT and DfX principles
- Strategic relevance in modern chip design cycles
- Key business drivers: yield, test cost, quality, time-to-market
- Overview of DfT techniques: Scan, BIST, LBIST, MBIST, JTAG, Boundary Scan
- Mapping DfT in the product lifecycle
- Fault models & test coverage
- DfT architecture trade-offs (area, performance, power, routing)
- Roles & responsibilities across design, verification, DfT, and ATE teams
- Wrap-up & open Q&A

Day 2: Execution, Challenges & Management Best Practices

- DfT project planning: milestones, dependencies, review points
- DfT flow & toolchain integration
- ATE & production test considerations
- Cost & ROI of DfT/DfX
- Quality metrics: defect coverage, yield loss, test escapes
- Common pitfalls & mitigation strategies
- Managing cross-team collaboration (Agile, Waterfall, hybrid)
- Final panel: expert Q&A and action plan

INSTRUCTOR

DFT expert with over 25 years of experience in product development with companies like
Apple, Intel, Philips and NXP Semiconductors. Has led chip development projects across
Europe, USA and Asia. Trained several engineers and managers on DfT topics.

INSTRUCTOR

Before attending, we recommend

- Preparing any questions related to this course.

ASSESEMENT

The following assessment activities are available to participants

- Participants who attend the full course will receive a SilTest Academy certificate of attendance.
- There will be a multiple-choice end of course test

REGISTER NOW!