MASTER ATE PLATFORMS FOR REAL-WORLD CHIP TESTING

Overview

A 2-week immersive training designed to give engineers and technicians the hands-on skills to operate leading Automated Test Equipment (ATE) platforms.

Work directly with Advantest (V93K, T2000), Teradyne (UltraFLEX, J750, ETSxx), or Chroma systems, covering both hardware and software essentials for real-world chip testing.

📌 Learn what it takes to succeed as a semiconductor test engineer.

Target Audience

- Test engineers and technicians
- QA professionals in semiconductor manufacturing
- Production engineers optimizing test processes
- New graduates or professionals transitioning into testing roles
- Engineers learning Advantest, Teradyne, or Chroma
- Managers overseeing test operations

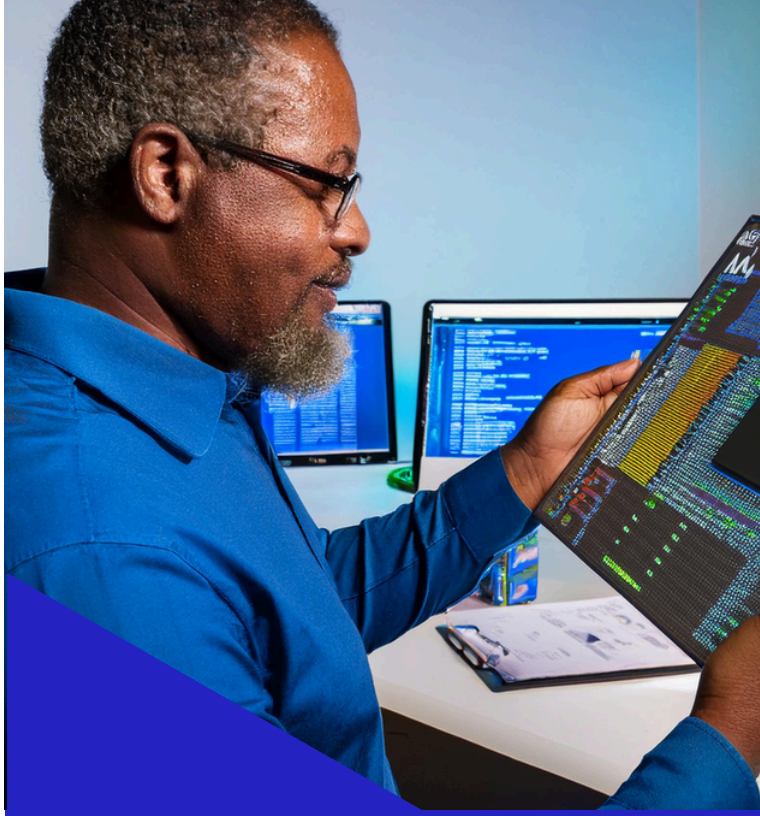
OBJECTIVES

By the end of this course, participants will be able to:

- Understand the architecture of major ATE platforms
- Create, debug, and validate production test programs
- Use shmoo plots, margin analysis, and diagnostic tools
- Configure digital, analog, and RF test modules
- Apply real-world debugging workflows from production floors

FORMAT & DELIVERY

- **Duration & Schedule:**
  1. **Intensive**: 2 weeks, 4 sessions/week, 4 hours/session
  2. **Flexible:** 8 weeks, 4 sessions/week, 2 hours/session (for working professionals)
- **Mode:** In-person or live online
- Format: Hands-on labs, interactive Q&A, group exercises
- **Materials:** Course slides, test files, and real-world case studies
- **Language:** English



CHIP TESTING USING ATES

COURSE CURRICULUM

Week 1: Foundations and Platform Familiarization

- ATE Architecture Overview (V93K, UltraFLEX, ETS-800, T2000, Chroma)
- Test Flow Concepts and Execution Engine Operation
- Test Pattern Creation, STIL/WGL basics
- ATE Instrument Integration and Calibration
- Introduction to Simulation, Debugging, and Test Setup

Week 2: Test Program Development, Debug, and Analysis

Module 1: Test Program Development

- Requirement Analysis & Test Strategy Planning
- Designing Test Architecture and Procedures
- Vector Generation, Instrument Integration, Programming Languages
- Test Execution, Validation, and Documentation

Module 2: Data Analysis & Debug

- Data Collection and Statistical Analysis
- Fault Diagnosis and Performance Characterization
- Yield Analysis, Root Cause Identification, SPC
- Debugging the Test Program: Tools, Code Review, and Iterative Testing

Module 3: Yield Optimization and Production Handoff

- Final Debug and Validation Loops
- Optimization Techniques to Reduce Test Time
- Characterization techniques and data correlation
- Case Study Exercises and Hands-On Debug Simulations
- Final Review and Certification Assessment

INSTRUCTOR

Delivered by SilTest senior ATE engineers and guest experts with deep experience across Advantest, Teradyne, Chroma, NI, and more.

Collectively, our team has built and debugged test programs for 100+ production chips at leading semiconductor companies.

INSTRUCTOR

Before attending, we recommend

- Preparing any questions related to this course.

ASSESEMENT

The following assessment activities are available to participants

- Participants who attend the full course will receive a SilTest Academy certificate of attendance.
- There will be a multiple-choice end of course test

REGISTER NOW!